IN THE SPECIFICATION

Please amend the Specification as follows:

At page 1, line 1, in the "CROSS REFERENCE TO RELATED APPLICATION" added by the preliminary amendment, please amend this section as follows:

"CROSS REFERENCE TO RELATED APPLICATION

This application claims the benefit and is a divisional of Application No. 09/749,074, filed December 27, 2000 by Zumkehr, et al, now ~~pending~~ issued as U.S. Patent No. 6,622,227."

Page 13, line 11, please amend the paragraph starting there-at and continuing through to page 14, line 17 as follows:

"Figure 3 is a block diagram of one embodiment of the translator hub 220 according to the teachings of the present invention. As shown in Figure 3, the translator hub includes a channel (also referred to as a main channel herein) that acts as an interface with the RAMUBS memory controller 210 and one or more channels (also referred to as branch channels herein) that act as an interface with the SDRAM devices 161. In one embodiment, the main channel ("RAMBUS INTERFACE") 310 is coupled to receive control signals, data signals, and clock signals from the RAMBUS memory controller 220 and to send the data signals to the RAMBUS memory controller 220. In one embodiment, the branch channels [[340]] ("SDRAM INTERFACE") 350 are coupled to send control, data, and clock signals to the SDRAM devices 161 and to

receive data from the SDRAM devices 161. The translator hub further includes a decode and SDRAM command generator unit 320 that decodes the commands received from the RAMBUS memory controller 210 via the main channel ("RAMBUS INTERFACE") 310 and generates the appropriate SDRAM commands based upon the decoded commands. The SDRAM commands generated are sent to the SDRAM devices 161 via the branch channels ("SDRAM INTERFACE") 350. As shown in Figure 3, the translator hub also includes data write buffers 330 to store write data received from the RAMBUS memory controller 210. As described herein, the buffered write data and the buffered write commands are sent to the SDRAM devices 161 for execution on a first-in-first-out basis when a new write command is received from the RAMBUS memory controller 210 without waiting for the write data for the new write command. The translator hub further includes a read data packetizer unit 340 to convert data received from the SDRAM devices 161 via the branch channels ("SDRAM INTERFACE") 350 into main channel data packets to be sent to the RAMBUS memory controller 210."